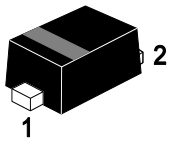
Transient Voltage Suppressors for ESD Protection

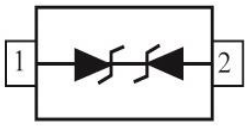
FEATURES:

- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- Peak power up to 200 Watts @ 8 x 20 _s Pulse
- ESD rating of Class 3 (> 16 kV) per Human Body Model
- Small body outline dimensions
- Low leakage
- Response time is typically < 1.0 ns
- IEC61000−4−2 level 4 ESD protection
- IEC61000−4−4 Level 4 EFT protection

Circuit Diagram & Pin Configuration:



SOD-523



DEVICE MARKING AND ORDERING INFORMATION

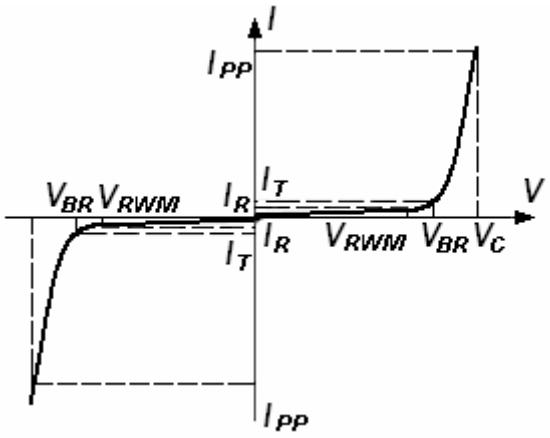
Device	Marking	Shipping
TESDN051BD52	5C	3000/Tape&Reel

MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
IEC 61000−4−2 (ESD) Contact Air		±8 ±15	kV
IEC 61000 - 4 - 4 (EFT)		40	kV
ESD Voltage(Per Human Body Model)		16	kV
Peak Pulse Power (tp = 8/20μs)	PPP	200	W
Maximum Junction Temperature	TJ	150	ºC
Operating Temperature Range	TOP	−55～+150	ºC
Lead Solder Temperature − Maximum (10 Second Duration)	TL	260	ºC
Storage temperature	Tstg	−55～+155	°C

Electrical Parameter

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
I_T	Test Current
V_{BR}	Breakdown Voltage @ I_T



●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

Device	VRWM (V)	IR (u A) @VRWM	VBR (V) @ IT (Note 1)		IT	VC (V) @Ipp = 5 A	VC (V) @Max Ipp	IPP(A)	PPK(W)	C (pF)
	Max	Max	Min	Max	mA	Max	Max	Max	Max	Typ
TESDN051BD52	5	1	5.6	7.8	1	11.6	18.6	9.4	174	25

1. VBR is measured with a pluse test current IT at an ambient temperature of 25℃.

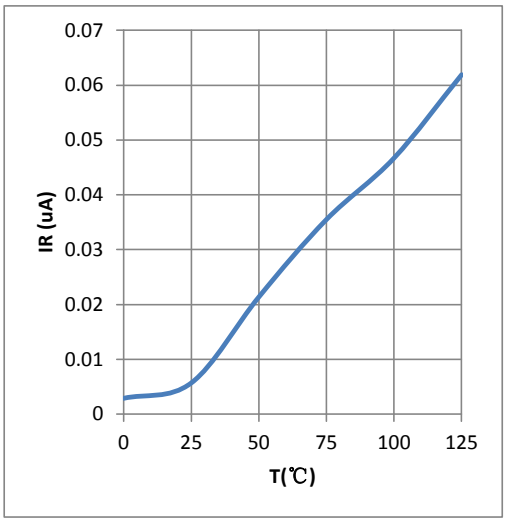


Fig 1. Reverese character

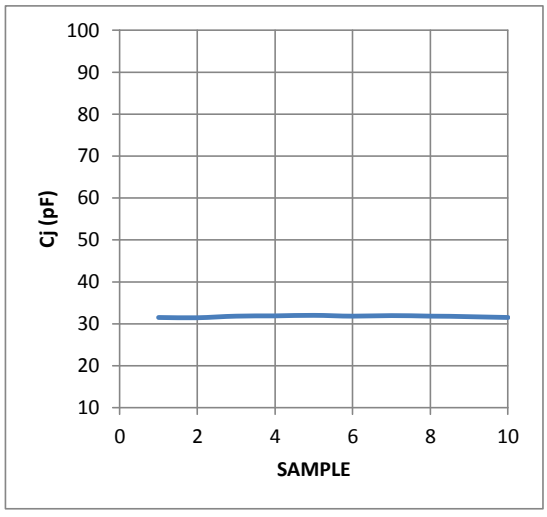


Fig 2. Capacitance character

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

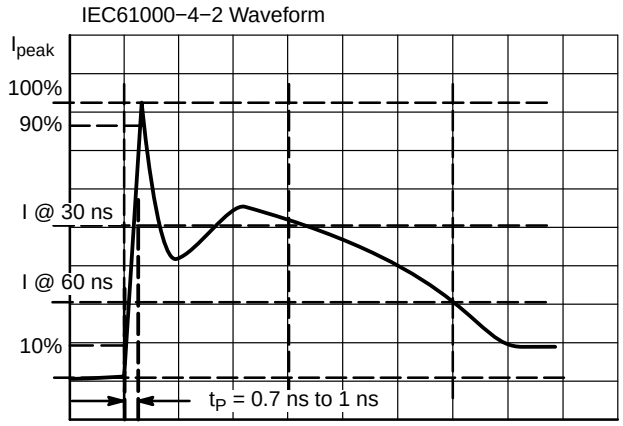


Figure 3. IEC61000−4−2 Spec

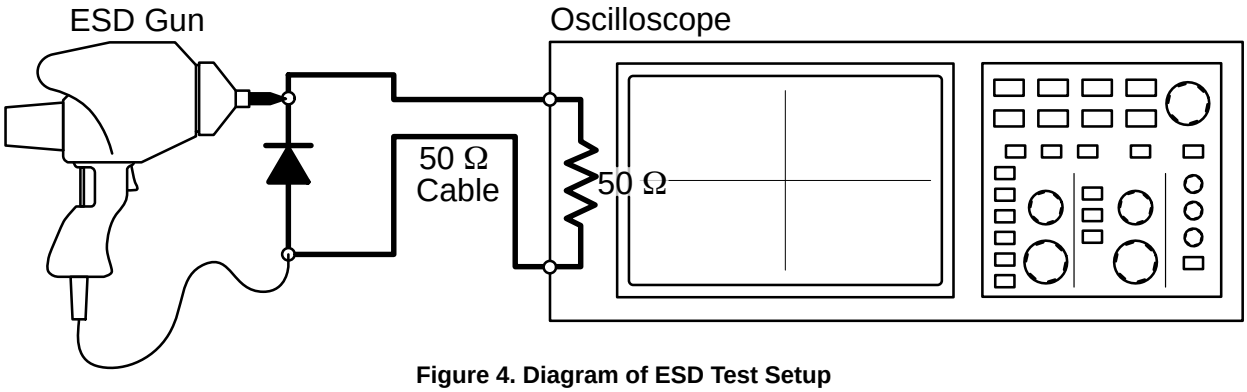


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level.

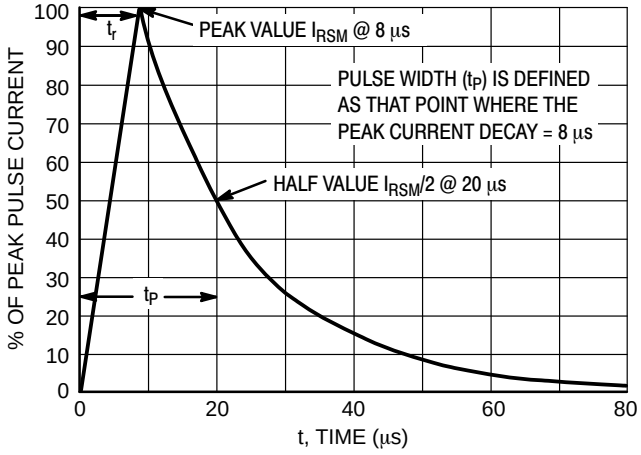
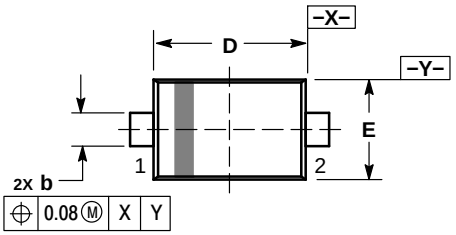


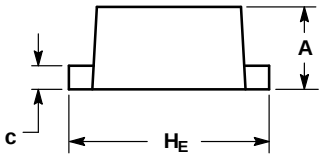
Figure 5. 8 X 20 μs Pulse Waveform

PACKAGE DIMENSIONS

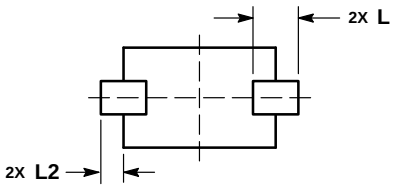
SOD−523



TOP VIEW



SIDE VIEW



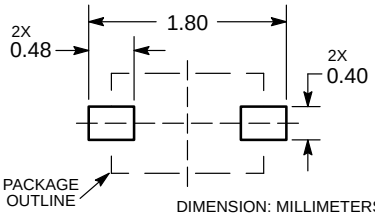
BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.07	0.14	0.20
D	1.10	1.20	1.30
E	0.70	0.80	0.90
H_E	1.50	1.60	1.70
L	0.30 REF		
L2	0.15	0.20	0.25

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

NOTICE

The information presented in this document is for reference only. Tinysemi reserves the right to make changes without notice for the specification of the products displayed herein.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Tintsemi elec Co., Ltd., or anyone on its behalf, assumes no responsibility or liability for any damagers resulting from such improper use of sale.

This publication supersedes & replaces all information reviously supplied. For additional information, please visit our website http://www.tinysemi.com , or consult your nearest Tinysemi’ s sales office for further assistance.