Transient Voltage Suppressors for ESD Protection

FEATURES:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
  0.039″ x 0.024″ (1.00 mm x 0.60 mm)
- Low Body Height: 0.016″ (0.4 mm)
- Stand−off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- This is a Pb−Free Device

Circuit Diagram & Pin Configuration:

SOD-923

PIN 1. CATHODE
2. ANODE

DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
TESDL051AD92	D	8000/Tape&Reel

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	150	mW
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature Range	T_J	−55 to +125	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

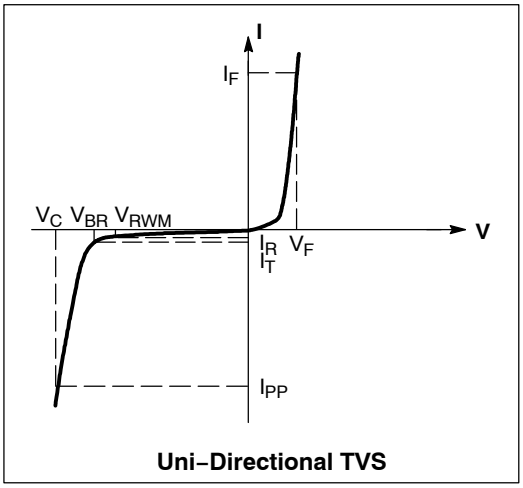
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.62 in.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.0 V Max. @ I_F = 10 mA for all types)

Device	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF)		V_C (V) @ I_{PP} = 1 A (Note 3)	V_C
	Max	Max	Min	mA	Typ	Max	Max	Per IEC61000−4−2 (Note 4)
TESDL051AD92	5.0	1.0	5.4	1.0	0.5	0.9	9.8	Figures 1 and 2 See Below

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Surge current waveform per Figure 5.
4. For test procedure see Figures 3 and 4.

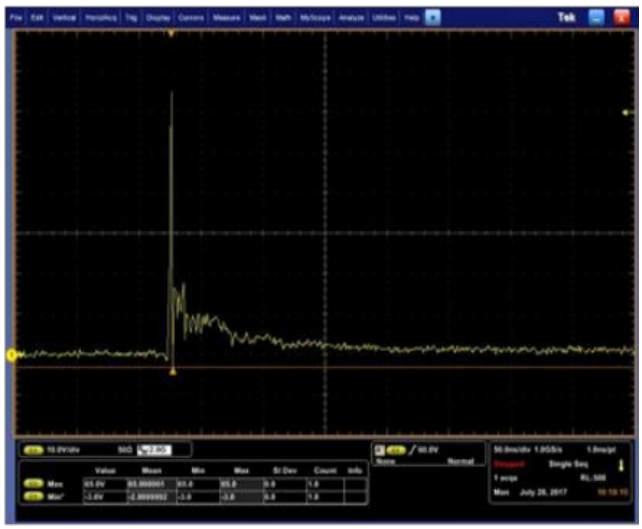


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

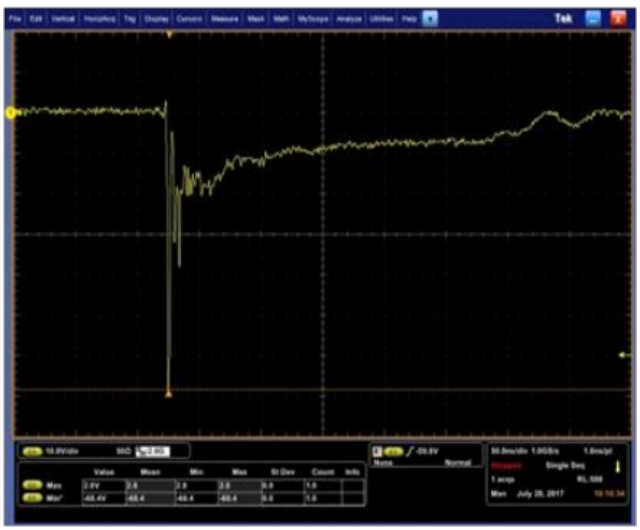


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

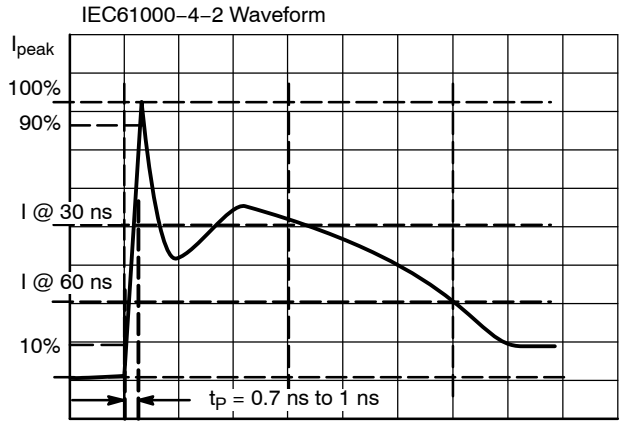


Figure 3. IEC61000−4−2 Spec

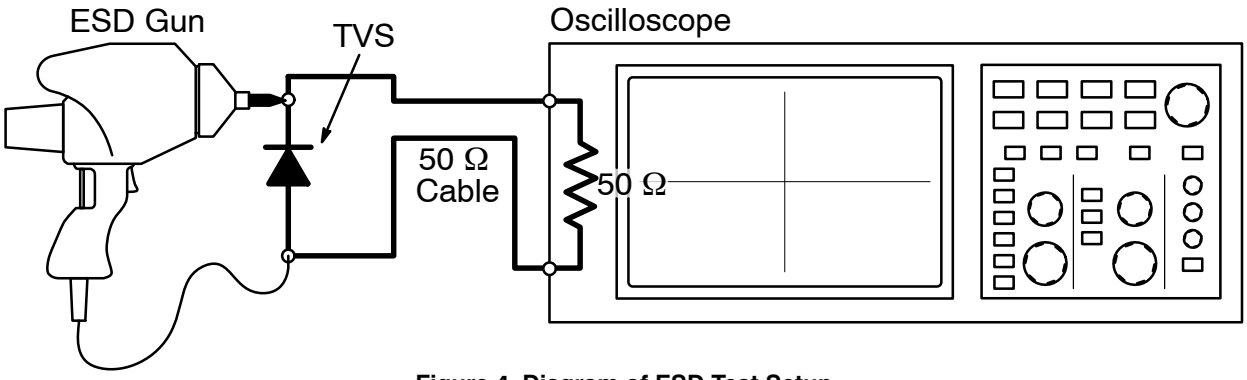


Figure 4. Diagram of ESD Test Setup

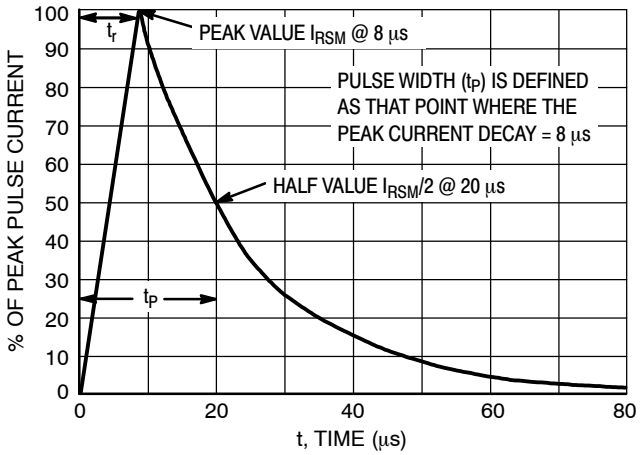
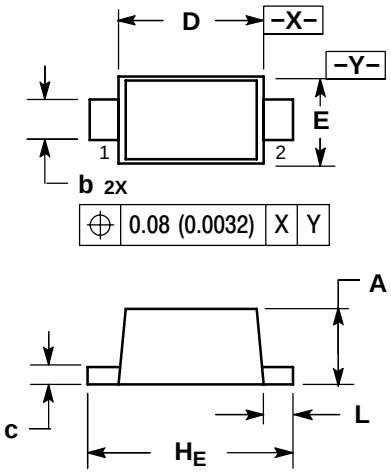


Figure 5. 8 X 20 μs Pulse Waveform

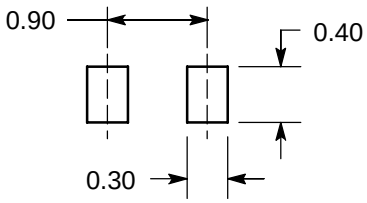
SOD−923



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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